PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of	Docket No: Q77183
Jae-jun MOON, et al.	
Appln. No.: 10/777,097	Group Art Unit: 2816
Confirmation No.: 4555	Examiner: Jeffery Shawn Zweizig
Filed: February 13, 2004	

For: BIAS CIRCUIT HAVING START-UP CIRCUIT

REPLY BRIEF PURSUANT TO 37 C.F.R. § 41.41

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.41, Appellant respectfully submits this Reply Brief in response to the Examiner's Answer dated August 3, 2007. Entry of this Reply Brief is respectfully requested.

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STATUS OF CLAIMS

Claims 1-10 are all the claims pending in the application. Claim 4 is objected to for reciting "a second common node" on line 13, when the claim should recite --the second common node--.

Claims 1,3 and 5-9 are rejected under 35 U.S.C. § 102(b) as being anticipated by Wu et. al (U.S. Patent No. 5,307,007; hereinafter "Wu").

Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 5,180,967; hereinafter "Yamazaki") in view of Wu.

Claims 1-10, which have been at least twice rejected, are the claims on appeal (See Claims Appendix).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on appeal are:

1. Claims 1, 3 and 5-9 are rejected under 35 U.S.C. § 102(b) as being anticipated by Wu et al. (U.S. Patent No. 5,307,007; hereinafter "Wu").

2. Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 5,180,967; hereinafter "Yamazaki") in view of Wu.

ARGUMENT

In the Appeal Brief, the Appliacant argued that Wu fails to disclose or suggest a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and a start-up circuit part having a capacitor connected between the output node and a common node the bias circuit and the start-up circuit, as recited in claim 1. Specifically, Appellant argued:

> In the Final Office Action, the Examiner states that the node between the NMOS transistors M1 and M3 corresponds to the claimed output node. See paragraph 2 at page 2. First, this particular node at the gate of NMOS transistor M3 cannot correspond to the claimed output node.

In part, the Appellant explained that this particular node is merely connected to the gate of the NMOS transistor M3, the gate of the NMOS transistor M4, the capacitor C_1, and the gates of transistors M5 and M6.[1] The Applicant further argued that:

[1] In response to Examiner's comments re incorrect statements of the Applicant, Applicant clarifies that this "particular node" is connected to the gate of the PMOS transistor M1 *through the capacitor* C_1. In addition, Applicant notes that the Examiner may be correct in stating that this "particular node" is not connected to the source/drain of M4. Upon further review of Fig. 1, Applicant notes that may be no node between the source of M4 and the gate of M3. At any rate, Applicant submits that the existence of a node between the source of M4 and the gate of M3 is not pertinent to Applicant's arguments.

Therefore, there the gate of MOS transistor M3 does not provide any sort of output, and thus, cannot possibly correspond to the claimed output node.[2]

Applicant points out that in a description of an embodiment of the invention, "an output voltage Vgn is outputted through the output node." Paragraph 43 of Specification and Fig. 7. In contrast, there is absolutely nothing at the gate of the NMOS transistor M3 which would allow the output or the detection of any voltage at the gate.

Second, the Examiner's argument that the gate of M3 corresponds to the claimed output node ignores the recitations of claim 1. In claim 1, the start-up

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[2] In the Examiner's Answer, the Examiner stated that "gates do not provide outputs," and that the "Examiner never suggested that the gate of M3 provides an output signal." Page 6. The Applicant, however, notes that in the Response to Arguments portion of the Final Office Action of August 30, 2005, the Examiner stated (bolded emphasis added):

> In reference to Applicants' arguments regarding the 102 rejection to claim 1, **the output from the gate of M3** (Fig. 1) is an output of the circuit M1-M4, R1 and C. . . . . Likewise, **the output from the gate M4** (Fig. 3) is an output of the circuit M3-M8, R1, C1 and C2.

> circuit part is recited as having a common node of in common connecting gates of MOS transistors and separately recites an output node to which a constant bias voltage is generated. In other words, the gate of M3 may correspond to a type of a common node, but does not correspond to an output node. Therefore, the characterization of the gate of M3 as corresponding to the claimed output node ignores the fine distinctions made by the Applicants in the claim language.
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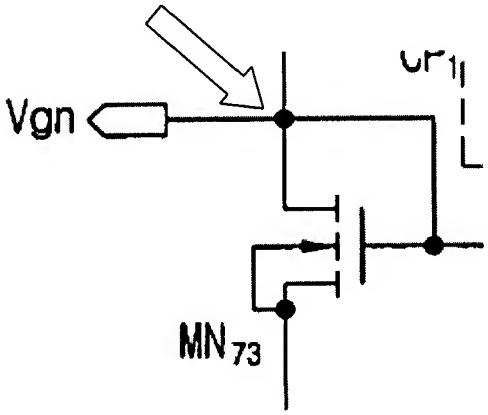
> (Appeal Brief, page 8.)

In the Examiner's Answer, the Examiner continues to take the position that:

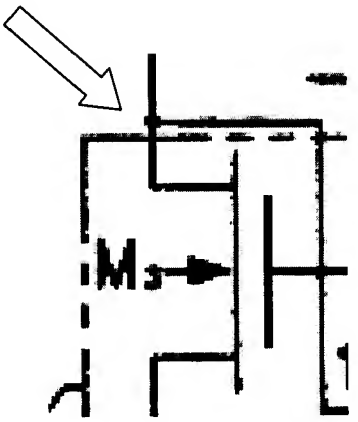
> In any event, as pointed out in the rejection above, Wu et al. Fig. 1 is seen to show an "output node" at the connection of transistors M1 and M3. This connection is called a node. The node connection between transistors M1 and M3 provides or outputs a constant bias voltage signal that is extracted by the gates of transistors M5 and M6, for example. Those of ordinary skill in the art would reasonably refer to such a connection configuration as an "output node".

Applicant disagrees because the node connection between the transistors M1 and M3 provides a signal to a node connected to the gate of transistor M3, and then, the signal is provided from the

gate of the transistor M3, to the gates of transistors M5 and M6. Reproduced below are annotated portions of Fig. 7 of Applicant's specification and Fig. 1 of Wu which show that Wu does not have an output node as alleged by the Examiner.



Portion of Fig. 7 of Applicant's invention



Portion of Fig. 1 of Wu

Give the differences above, we disagree with the Examiner's statement that:

> **node of the Wilson-type bias sub-circuit. The output node between bias circuit transistors M1 and M3 is exactly the same as the output node REF or Vgn shown in Appellant's Fig. 1 or 7, respectively.**

P. 7 of Examiner's Answer.

Applicant further submits that in the current state of patent law and practice, an Applicant is allowed to be his own lexicographer. The Applicant's definition of the term has been made substantially of record both in this response as well as in earlier responses to Office Actions. Therefore, the Examiner's attempt to stretch the definition to somehow read on Wu is believed to be unreasonable.

As for Yamazaki, the Examiner states that:

> component 116, for example. Although the node N11 is internal to the larger electronic system, the node is, nevertheless, an output node of the Wilson-type bias sub-circuit.

Page 9, Examiner's Answer. We disagree.

Assuming arguendo, that the circuit in Fig. 1 of Yamazaki can be modified to include the capacitor C1 of Wu, the Examiner has not shown how such a combination would disclose a start-up circuit part having **a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors** constructing the current mirror circuit. In other words, the Examiner has not shown how the capacitor C1 would be connected between the node N11 and the common node connecting gates of PMOS transistors 104 and 106. Rather, the capacitor C1 would be connected between the common node connecting gates of NMOS transistors 112 and 110 and the common node connecting gates of PMOS transistors 104 and 106.

As for node N12 of Yamazaki, the Examiner states that "if a usable signal is available at a node, than that node is an "output node." Page 9. We also disagree because the Examiner is unreasonably stretching the definition of "output node" beyond the Applicant's definition of the term. In Yamazaki, the node N12 is connected to the transistor 120. Rather than outputting a signal, Fig. 1 shows the node N12 **receiving** I_b from the transistor 120 and the power supply VDD.

Furthermore, the Examiner has not shown how N12 would output a constant bias voltage, as recited in claim 1. Rather, the connection of the node N12 to the power supply VDD through

the transistor 120. Assuming *arguendo*, that N12 receives voltage from the power supply VDD, through the transistor 120, the voltage received at the node N12 would include the noise existing in the power supply VDD and thus, the voltage at node N12 would not output a constant bias voltage. *See* paragraph 9 of Applicant's Specification ("such a circuit has a drawback in that noise existing on a power source voltage and the like is coupled with the bias voltage V_{REF} through the resistor R_{22} and the capacitor C_{21} and thus affect the bias voltage V_{REF}.").

In the Answer, the Examiner also alleges that:

> Beginning at the top of page 15, Appellant argues that Yamazaki may not generate a constant bias voltage. The portion of Appellant's circuit structure relevant to generating a constant bias voltage is identical to Yamazaki's structure relavant to generating a constant bias voltage. If Appellant's structure generates a constant bias voltage than the corresponding structure of the Yamazaki circuit must also generate a constant bias voltage. Appellant argues that Yamazaki may not offer an improvement

Applicant disagrees in that the Examiner is ignoring the additional components that are shown in Fig. 1 of Yamazaki. Yamazaki additionally discloses transistors 116, 118 and 120 which are not shown in Fig. 7 of Applicant's invention. These transistors 116, 118 and 120 **must** affect the operation of circuit A of Yamazaki, and therefore, the Examiner's presumption that node N12 of circuit A would provide a constant bias voltage, is without support.

CONCLUSION

For the above reasons as well as the reasons set forth in Appeal Brief, Appellant respectfully requests that the Board reverse the Examiner's rejections of all claims on Appeal.

An early and favorable decision on the merits of this Appeal is respectfully requested.

Respectfully submitted,

/ Seok-Won Stuart Lee /

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Date: **October 3, 2007**